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10ELN15/25

First/Second Semester B.E. Degree Examination, Dec.2016/Jan.2017
Basic Electronics

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, choosing at least two from each part.***

PART – A

1 a. Choose the correct answers for the following : **(04 Marks)**

i) When a diode is heavily doped
A) the leakage current will be low B) the zener voltage will be low
C) the depletion region will be thin D) the depletion region will be wide.

ii) A high reverse voltage applied to a junction diode will cause an effect known as
A) Punch through B) Avalanche breakdown
C) Diffusion D) Saturation.

iii) Zener diode regulates only when it is connected in
A) forward bias B) No bias C) Short D) Reverse bias.

iv) An ideal diode is having _____ forward resistance.
A) zero B) medium C) high D) none of these.

b. For a full wave rectifier circuit with two diodes, derive the current expression for i) average value ii) rms value iii) Ripple factor iv) efficiency v) PIV. **(10 Marks)**

c. Design a voltage regulator using zener diode to meet the following specifications : Dc unregulated input is 20V, V_o = 10V, load current is 0-20mA, I_{2min} = 10mA, I_{2max} = 100mA. **(06 Marks)**

2 a. Choose the correct answers for the following : **(04 Marks)**

i) The arrow on the emitter of a transistor indicates
A) the direction of electron flow B) the ground connection
C) the positive voltage point D) the negative voltage point

ii) When a transistor is used as an amplifier, it is normally operated in ------- region.
A) Saturation B) cut off C) active D) diffusion.

iii) The relation for α_{dc} in terms of β_{dc} is
A) $\alpha_{dc} = \frac{1+\beta_{dc}}{\beta_{dc}}$ B) $\alpha_{dc} = \frac{1-\beta_{dc}}{\beta_{dc}}$ C) $\alpha_{dc} = \frac{\beta_{dc}}{1-\beta_{dc}}$ D) $\alpha_{dc} = \frac{\beta_{dc}}{1+\beta_{dc}}$

iv) Find I_E of a transistor with I_c = 5.25mA and I_B = 100μA
A) 5.53mA B) 5.35mA C) 6.35mA D) 4.53mA

b. Draw the PNP transistor circuit in CB configuration. Sketch the output characteristics. Indicate active, saturation and cutoff regions. Briefly explain the nature of these curves. **(10 Marks)**

c. For the CE circuit shown in Fig Q2(c). Draw the dc load line and mark the dc operating point on it Assume β = 100 and neglect V_{BE}. **(06 Marks)**

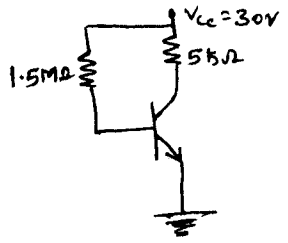

Fig Q2(c)

3 a. Choose the correct answers for the following : **(04 Marks)**

i) The biasing circuit, which gives most stable operating points is

A) Fixed B) Collector C) Emitter D) Voltage divider

ii) The stability factor (s) for a given transistor is

A) $S = \frac{\Delta I_C}{\Delta I_{CBO}}$ B) $S = \frac{\Delta I_{CBO}}{\Delta I_C}$ C) $S = \frac{1}{\Delta I_{CBO}}$ D) $S = \frac{\Delta I_B}{\Delta I_{CBO}}$

iii) The voltage divider biasing circuit is also called as

A) Self Bias B) Emitter current Bias

C) Both A and B D) None of these.

iv) In a transistor with normal bias, the emitter junction is

A) High resistance B) No bias C) Reverse biased D) Forward biased.

b. With neat circuit diagram, explain the working of an base bias circuit transistor and its design procedure. **(08 Marks)**

c. A voltage divider bias circuit with $V_{CC} = 20V$ and $R_C = 6k\Omega$ uses a transistor with $\beta = 80$, calculate suitable resistor values to give $V_{CE} = 8V$, $V_E = 5V$. Assume $V_{BE} = 0.7V$. **(08 Marks)**

4 a. Choose the correct answers for the following :

i) A Silicon controlled Rectifier is a _____ layer device

A) Two B) Three C) Four D) None of these.

ii) The region between peak point and valley point in VI characteristics of UJT is called __.

A) cut off region B) active region

C) Negative resistance region D) Saturation region.

iii) When JFET is operated above pinch off voltage its drain current.

A) Becomes zero B) Starts decreasing

C) Increases sharply D) Becomes constant.

iv) The function of gate in SCR is to control the

A) voltage regulation B) Flow of current

C) voltage amplification D) All of these. **(04 Marks)**

b. Draw and explain and VI characteristics of SCR. **(08 Marks)**

c. Draw the typical drain characteristics of P-channel JFET and indicate various regions and explain. **(08 Marks)**

PART – B

5 a. Choose the correct answers for the following :

i) The advantages of negative feedback is

A) to stabilize the voltage gain B) to increase the bandwidth

C) to reduce phase shift distortion D) All of these.

ii) In case of RC phase shift oscillator, the RC network produces a phase shift of

A) 90° B) 270° C) 180° D) 360°

iii) The objective of using a crystal oscillator is to get

A) 50 to 70Hz B) stable frequency

C) Variable frequency D) none of these.

iv) Which of the following oscillator is used to generate high frequencies?

A) RC phase shift B) Wein bridge

C) L.C oscillator D) Colpitts oscillator. **(04 Marks)**

b. With a neat circuit diagram, explain the working of a two stage capacitor coupled CE amplifier. **(08 Marks)**

c. With a neat circuit diagram, explain the working of Hartley oscillator. State the condition for oscillations. **(08 Marks)**

6 a. Choose the correct answers for the following :

i) The common mode rejection ratio of an ideal op-amp is

A) zero B) low C) high D) infinite

ii) The differential amplifier has

A) one input and one output B) two inputs and two outputs

C) two inputs and one output D) one input and two outputs

iii) -------- converts physical quantity to electrical signal

A) Amplifier B) Transducer C) Modulator D) Transmitter.

iv) What is the output voltage of an inverting amplifier, if the input voltage is 0.2V and $R_1 = 20K\Omega$, $R_f = 200K\Omega$.

A) 2V B) -10V C) 20V D) -2V **(04 Marks)**

b. Draw the following circuits using inverting op-amp and derive its output voltage

i) Adder ii) Integrator. **(10 Marks)**

c. Draw the block diagram of a CRO and explain the function of each block. **(06 Marks)**

7 a. Choose the correct answers for the following : **(04 Marks)**

i) The expression for modulation index in terms of carrier power and total power in an AM wave is

A) $m_a = \sqrt{2\left(\frac{pt}{pc} - 1\right)}$ B) $m_a = \sqrt{2\left(\frac{pt}{pc} - 1\right)^2}$ C) $m_a = \sqrt{\left(\frac{pt}{pc} - 1\right)}$ D) None of these.

ii) What is the 2's complement value of $15_{(16)}$

A) 0001 B) 0000 C) 0100 D) 1000.

iii) The Hexadecimal number A9, its equivalent value in binary

A) 10011010 B) 10101001 C) 10001001 D) 10100101.

iv) $35_{(10)} + 26_{(8)}$ in binary is

A) 001101 B) 111001 C) 110010 D) 100100.

b. Explain the need for modulation. **(04 Marks)**

c. A carrier of 1MHz with 400w of power is amplitude modulated with a sinusoidal signal of 2500Hz. The depth of modulation is 75% calculate the sideband of frequency bandwidth and power in sidebands and total power in modulated wave **(06 Marks)**

d. Solve the following :

i) $[0.7642]_{10}$ = ---------- (2) ii) $[AD6CB]_{16}$ = --------- (8) iii) $[11011.1011]_2$ = --------- 8

iv) Add $(BCD)_{16}$ to $(F89)_{16}$ v) Subtract using 8's complement method $66_{(8)} - 64_{(8)}$

vi) Subtract using 1's complement method $1010.001_{(2)} - 100.11_{(2)}$ **(06 Marks)**

8 a. Choose the correct answers for the following : **(04 Marks)**

i) NAND gate is a combination of ------ and --------.

A) AND and OR B) OR and NOT C) AND and NOT D) None of these.

ii) A logic gate is having ------- Number of inputs.

A) 1 B) 2 C) 3 D) 1 or more

iii) For which gate, when the two inputs A and B are equal the output is one and otherwise zero.

A) AND B) NOT C) EX-NOR D) EX-OR

iv) Simplified form of Boolean expression $(A+B)\cdot(A+C)$ is

A) AB+C B) $\overline{A} + BC$ C) A+BC D) A+B+C.

b. Draw the logic circuit for full adder and write its truth table with expression. **(08 Marks)**

c. Simply the following Boolean expressions and realize them using NAND gates.

i) $F(X, Y, Z) = X\overline{Y}\,\overline{Z} + \overline{X}\,\overline{Y}\,\overline{Z} + \overline{X}\,\overline{Y} + X\,\overline{Y}$

ii) $F(X, Y, Z) = \overline{(X + \overline{Y}\,Z)(\overline{X} + \overline{Y} + \overline{Z})(\overline{X} + Y)}$ **(08 Marks)**